Image AF/2811

OIPE JC26
JAN 29 2004
PATENT & TRADEMARK OFFICE

Docket No.: GR 97 P 6457

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

MAIL STOP: APPEAL BRIEF-PATENTS

By: _____ Date: January 26, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

| | | |
|---|---|---|
| Applic. No. | : | 09/595,860 Confirmation No.: 2756 |
| Inventor | : | Jörg Berthold et al. |
| Filed | : | June 16, 2000 |
| Title | : | Integrated Circuit Having a Diffusion Blocker Configured as a Blocker Layer and Connection Pieces Composed of Aluminum Covering Contact Holes and Methods for Fabricating the Same |
| TC/A.U. | : | 2811 |
| Examiner | : | Cuong Q. Nguyen |
| **Customer No.** | **:** | **24131** |

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

# BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office action dated September 10, 2003, finally rejecting claims 1-23 and 27.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $330.00 to cover the fee for filing the *Brief on Appeal*.

02/02/2004 MAHMED1 00000018 09595860
01 FC:1402 330.00 OP

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-23 and 27 are rejected and are under appeal. Claims 25-26 were cancelled in an amendment filed July 1, 2002. Claims 24 and 28 are withdrawn from further consideration.

Status of Amendments:

No claims were amended after the final Office action. A *Notice of Appeal* was filed on November 24, 2003.

Summary of the Invention:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention relates to an integrated electrical circuit having a plurality of structure planes, in which electrically active elements are situated on at least one element structure plane. At least

one insulation layer is disposed above the element structure plane and electrical connecting leads are disposed within and/or above the insulation layer. At least a portion of the connecting leads contains so much copper that copper is predominant for the properties of the connecting leads, and at least one diffusion blocker is disposed underneath the connecting leads, which diffusion blocker impedes and/or prevents the diffusion of copper.

Appellants explained on page 15 of the specification, line 10, that in all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown an integrated electrical circuit having field-effect transistors 20, 30 and 40 that are situated on a semiconductor substrate 10 preferably composed of silicon. The field-effect transistors 20, 30 and 40 each have source and drain regions 50, 60, 70, 80, 90 and 100 and also gate electrodes 120, 130 and 140.

Appellants further explained on page 15 of the specification, line 21, that an insulation layer 150 is situated between the field-effect transistors 20, 30 and 40 and also above the source and drain regions 50, 60, 70, 80, 90 and 100 and also

between the gate electrodes 120, 130 and 140. The insulation layer 150 may be formed, in particular, by an intermediate oxide, for example a flowable planarization oxide such as borophosphorus silicate glass (BPSG). The intermediate oxide can be replaced by any other insulating material. However, the use of borophosphorus silicate glass has the particular advantage that, on account of its flowability, it may be possible to dispense with a process of chemical mechanical planarization for the purpose of producing a planar surface.

It is outlined on page 16 of the specification, line 8, that a blocker layer 160 having a thickness of 150 nm and made, for example, of silicon oxynitride SiON is disposed above the insulation layer 150. The blocker layer 160 is disposed above the entire surface of the semiconductor substrate 10 and is interrupted only in a region of contact holes 170, 180, 190, 200, 210 and 220. The contact holes 170, 180, 190, 200, 210 and 220 are preferably filled in a whole-area manner with a conductive material, for example a metal, preferably tungsten or a tungsten alloy.

It is also outlined on page 16 of the specification, line 18, that, as can be discerned from Fig. 2, an adhesion layer 165 having a thickness of approximately 100 nm and made of a titanium/titanium nitride alloy is situated between a tungsten

filling 230 of a contact hole 240 and the layers which bound the contact hole, that is to say the insulation layer 150 and the blocker layer 160. The adhesion layer 165 serves as a seeding layer for subsequent deposition operations, in particular for the filling of the contact holes 170, 180, 190, 200, 210, 220 and 240 with tungsten, for example. In addition, the adhesion layer 165 protects the material underneath the bottom of the contact hole.

It is set forth on page 17 of the specification, line 4, that above the contact holes 170, 180, 190, 200, 210, 220 and 240, connection pieces 250, 260, 270, 280, 290, 300 and 310 are situated directly on the blocker layer 160. The connection pieces being made of a material which combines a high conductivity with a minor diffusion tendency, for example aluminum.

Appellants also set forth on page 17 of the specification, line 11, that a further insulation layer 320, which is also referred to as an intermetal oxide, is situated above and between the connection pieces 250, 260, 270, 280, 290, 300 and 310. However, it is not necessary for the insulation layer 320 to be composed of an oxide, although it is technologically particularly expedient for it to be composed of a semiconductor oxide such as, for example, $SiO_2$ formed by a TEOS

(tetraethyl orthosilicate = $SiO(OC_2H_5)_4$) method. As an alternative, it is possible for the insulation layer 320 (that is to say the intermetal oxide in this case) to be deposited for example by a chemical vapor deposition (CVD) method. In all of the cases mentioned, the production of the insulation layer 320 can be integrated without difficulty in the process for fabricating the electrical circuit.

Appellants outlined on page 18 of the specification, line 1, that contact holes 330, 340, 350, 360 and 370 are likewise etched into the insulation layer 320.

Appellants further outlined on page 18 of the specification, line 4, that the contact holes 330, 340, 350, 360 and 370 are filled with tungsten or copper in a whole-area manner. Above the insulation layer 320, connection pieces 390 and 400 and also an interconnect 410 made of copper are situated in a further insulation layer 380.

It is also stated on page 18 of the specification, line 10, that contact holes 420 and 430 are likewise situated in the insulation layer 380 and are in turn filled with tungsten or copper in a whole-area manner.

Appellants also explained on page 18 of the specification, line 14, that connection pieces 440 and 450 made of copper are likewise disposed above the contact holes 420 and 430. The connection pieces 440, 450 are situated in an intermetal dielectric 460 which lies above the insulation layer 380 and is composed of a silicon oxide $SiO_2$, for example.

Appellants outlined in the last paragraph on page 18 of the specification, line 20, that the integrated electrical circuit of this type can be produced in the manner explained below. The field-effect transistors 20, 30 and 40 with the source and drain regions 50, 60, 70, 80, 90 and 100 and also with the gate electrodes 120, 130 and 140 are fabricated in a known manner in the region of a main area of the semiconductor substrate 10.

Appellants outlined on page 19 of the specification, line 1, that this is followed by the production of the insulation layer 150, for example by the flowing of a flowable planarization oxide such as borophosphorus silicate glass (BPSG) or by a coating method such as plasma-enhanced CVD: PECVD (plasma enhanced chemical vapor deposition) method.

Appellants further outlined on page 19 of the specification, line 7, that the blocker layer 160 having a thickness of

approximately 100 nm is coated onto the insulation layer 150. The blocker layer 160 - for example made of silicon oxynitride SiON - may preferably be fabricated by a PECVD method. A significant advantage of the PECVD method is that it can be carried out even at temperatures of below 500° C. In this case, free radicals are produced in a plasma. These are silicon, oxide and nitride radicals in the case of an SiON layer being deposited. Silane ($SiH_4$), ammonia ($NH_3$) and oxygen are used for carrying out the method. The blocker layer 160 is deposited at a pressure in the range of from about 20 to 100 Pa, preferably approximately 30 Pa, and a temperature below 500° C, preferably about 300° C.

It is set forth in the last paragraph on page 19 of the specification, line 21, that, afterwards, the contact holes 170, 180, 190, 200, 210, 220 and 240 are etched into the insulation layer 150 and into the blocker layer 160, preferably by a dry etching method in a reactive plasma. An example of an etchant used is a gas mixture comprising $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$.

Appellants stated on page 20 of the specification, line 1, that the adhesion layer 165 having a thickness of approximately 100 nm and made of a titanium/titanium nitride alloy is subsequently deposited. The contact holes 170, 180,

190, 200, 210, 220 and 240 are thereupon filled with tungsten or copper.

Appellants further stated on page 20 of the specification, line 6, that the connection pieces 250, 260, 270, 280, 290, 300 and 310 that may also be connecting elements, are subsequently applied for example by the sputtering and subsequent patterning of a metal layer.

It is also set forth on page 20 of the specification, line 11, that a patterning process according to a conventional photolithographic method patterns that part of the adhesion layer 165 which lies above the blocker layer 160 and equally the connection pieces 250, 260, 270, 280, 290, 300 and 310.

As described on page 20 of the specification, line 16, the insulation layer 320 is then deposited onto the blocker layer 160 and the connection pieces 250, 260, 270, 280, 290, 300 and 310 by a suitable deposition method - such as plasma enhanced chemical vapor deposition (PECVD).

Appellants described in the last paragraph on page 20 of the specification, line 21, that the contact holes 330, 340, 350, 360 and 370 are then etched into the insulation layer 320 preferably by a dry etching method in a reactive plasma. An

example of a suitable etchant used is a gas mixture containing $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$.

Appellants explained on page 21 of the specification, line 1, that the connection pieces 390 and 400 made of copper and also an interconnect 410, which serves for connecting the contact holes 350 and 360 and is likewise composed of copper, are produced in the manner explained below. A copper layer having a thickness of from 300 nm to 600 nm is applied to the layer 320 by a sputtering method. A resist mask is then applied and patterned by photolithographic process steps.

Appellants further explained on page 21 of the specification, lien 9, that the insulation layer 380 is subsequently applied. The contact holes 420 and 430 are then etched into the insulation layer 380 preferably by a dry etching method in a reactive plasma. An example of an etchant used is once again a gas mixture containing $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$. The contact holes 420 and 430 are subsequently filled with copper. The connection pieces 440 and 450 made of copper are then applied to the contact holes 420 and 430.

It is also stated on page 21 of the specification, line 18, that a further plane 460 formed for example by an intermetal dielectric such as $SiO_2$ is subsequently applied.

It is outlined in the last paragraph on page 21 of the specification, line 21, that, in the case of a second embodiment of the integrated electrical circuit illustrated in Fig. 3, field-effect transistors 520, 530 and 540 are situated on a semiconductor substrate 510 preferably composed of silicon. The field-effect transistors 520, 530 and 540 each have source and drain regions 550, 560, 570, 580, 590 and 600 and also gate electrodes 620, 630 and 640.

Appellants stated on page 22 of the specification, line 4, that an insulation layer 650 is situated between the field-effect transistors 520, 530 and 540 and also above the source and drain regions and also the gate electrodes. The insulation layer 650 may be composed, in particular, of an intermediate oxide, for example a flowable planarization oxide such as borophosphorus silicate glass (BPSG). The intermediate oxide may be replaced by any other insulating material. However, the use of borophosphorus silicate glass has the particular advantage that, on account of its flowability, it may be possible to dispense with a process of chemical mechanical planarization for the purpose of producing a planar surface.

Appellants set forth in the last paragraph on page 22 of the specification, line 16, that a blocker layer 660 having a thickness of 150 nm and made of silicon oxynitride SiON is disposed above the insulation layer 650. The blocker layer 660 is disposed above the entire surface of the semiconductor substrate 510 and encloses the connection pieces 750, 760, 770, 780, 790 and 800 located in the region of contact holes 670, 680, 690, 700, 710, 720 and 740. The contact holes 670, 680, 690, 700, 710 and 720 are preferably filled in a whole-area manner with a conductive material, for example a metal, preferably tungsten or a tungsten alloy. The connection pieces 750, 760, 770, 780, 790, 800 and 810 are composed of a material that combines a high conductivity with a minor diffusion tendency, for example aluminum.

Appellants explained on page 23 of the specification, line 4, that, as can be discerned from Fig. 4, an adhesion layer 665 having a thickness of approximately 100 nm and made of a titanium/titanium nitride alloy is situated between the tungsten filling 730 of a contact hole 740 and the layer which bounds the contact hole, that is to say in this case the insulation layer 650. The adhesion layer 665 serves as a seeding layer for subsequent deposition operations, in particular for the filling of the contact holes 670, 680, 690, 700, 710, 720 and 740 with tungsten, for example. In

addition, the adhesion layer 665 protects the material underneath the bottom of the contact hole.

It is set forth in the last paragraph on page 23 of the specification, line 16, that a further insulation layer 820, which is also referred to as an intermetal oxide, is situated above and between the connection pieces 750, 760, 770, 780, 790, 800. However, it is not necessary for the insulation layer 820 to be composed of an oxide, although it is technologically particularly expedient for it to be composed of a semiconductor oxide such as, for example, $SiO_2$ formed by a TEOS (tetraethyl orthosilicate = $SiO(OC_2H_5)_4$) method. As an alternative, it is possible for the insulation layer 820 (that is to say the intermetal oxide in this case) to be deposited for example by a chemical vapor deposition (CVD) method. In all of the cases mentioned, the production of the insulation layer 820 can be integrated without difficulty in the process for fabricating the electrical circuit.

Appellants explained on page 24 of the specification, line 5, that contact holes 830, 840, 850 and 860 are likewise etched into the insulation layer 820.

Appellants further explained on page 24 of the specification, line 8, that the contact holes 830, 840, 850 and 860 are

filled with tungsten or copper in a whole-area manner. Above the insulation layer 820, connection pieces 890 and 890 and also an interconnect 910 made of copper are situated in a further insulation layer 880.

It is also stated on page 24 of the specification, line 24, that contact holes 920 and 930 are likewise situated in the insulation layer 880 and are in turn filled with tungsten or copper in a whole-area manner.

Appellants also described on page 24 of the specification, line 18, that connection pieces 940 and 950 made of copper are likewise disposed above the contact holes 920 and 930.

It is set forth in the last paragraph on page 24 of the specification, line 21, that an integrated electrical circuit of this type can be produced in the manner explained below. The field-effect transistors 520, 530 and 540 with the source and drain regions 550, 560, 570, 580, 590 and 600 and also with the gate electrodes 620, 630 and 640 are fabricated in a known manner in the region of a main area of a semiconductor substrate 510.

Appellants outlined on page 25 of the specification, line 1, that this is followed by the production of the insulation

layer 650, for example by the flowing of a flowable planarization oxide such as borophosphorus silicate glass (BPSG) or by a coating method such as plasma-enhanced CVD: PECVD (plasma enhanced chemical vapor deposition) method.

Appellants further outlined on page 25 of the specification, line 8, that, afterwards, the contact holes 670, 680, 690, 700, 710, 720 and 740 are etched into the insulation layer 650, preferably by a dry etching method in a reactive plasma. An example of an etchant used is a gas mixture containing $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$.

It is also stated on page 25 of the specification, line 14, that the adhesion layer 665 having a thickness of approximately 100 nm and made of a titanium/titanium nitride alloy is subsequently deposited. The contact holes 670, 680, 690, 700, 710, 720 and 740 are thereupon filled with tungsten or copper.

Appellants described in the last paragraph on page 25 of the specification, line 19, that the connection pieces 750, 760, 770, 780, 790 and 800, which may also be connecting elements, are subsequently applied for example by the sputtering and subsequent patterning of a metal layer made of aluminum or an aluminum alloy, for example. A patterning process according

to a conventional photolithographic method patterns that part of the adhesion layer 665 which lies above the insulation layer 650 and equally the connection pieces 750, 760, 770, 780, 790 and 800.

Appellants outlined on page 26 of the specification, line 2, that the blocker layer 660 having a thickness of approximately 100 nm is then coated onto the insulation layer 650 and the connection pieces 750, 760, 770, 780, 790 and 800. The blocker layer 660 - for example made of silicon oxynitride SiON - may preferably be fabricated by a PECVD method. A significant advantage of the PECVD method is that it can be carried out even at temperatures of below 500° C. In this case, free radicals are produced in a plasma. These are silicon, oxide and nitride radicals in the case of an SiON layer being deposited. Silane ($SiH_4$), ammonia ($NH_3$) and oxygen are used for carrying out the method. The blocker layer 660 is preferably deposited at a pressure in the range of about 20 to 100 Pa, ideally at about 30 Pa, and a temperature of below 500° C, preferably about 300° C.

Appellants further outlined on page 26 of the specification, line 17, that the connection pieces 750, 760, 770, 780, 790 and 800 are subsequently produced by applying and subsequently patterning a metal layer. The insulation layer 820 is then

deposited onto the blocker layer 660 and the connection pieces 750, 760, 770, 780, 790, 800 and 810 by a suitable deposition method such as chemical vapor deposition (CVD). The contact holes 830, 840, 850, 860 and 870 are then etched into the insulation layer 820. An example of an etchant used is a gas mixture containing $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$.

It is set forth in the first paragraph on page 27 of the specification, line 1, that the connection pieces 890 and 900 made of copper and also an interconnect 910, which serves for connecting the contact holes 850 and 860 and is likewise composed of copper, are produced in the manner explained below. A copper layer having a thickness of from 300 nm to 600 nm is applied to the insulation layer 820 by a sputtering method. A resist mask is then applied and patterned by photolithographic process steps.

As further outlined on page 27 of the specification, line 9, the further insulation layer 880 is then deposited. The contact holes 920 and 930 are then etched into the insulation layer 880 preferably by a dry etching method in a reactive plasma. An example of an etchant used is again a gas mixture containing $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$. The contact holes 920 and 930 are subsequently filled with copper.

Connection pieces 940 and 950 made of copper are then applied to the contact holes 920 and 930.

Appellants stated in the last paragraph on page 27 of the specification, line 18, that the intermetal dielectric 960, for example made of silicon oxide $SiO_2$, is subsequently applied.

References Cited:

U.S. Patent No. 5,552,627 (McCollum et al.), dated September 3, 1996;

U.S. Patent No. 5,679,269 (Cohen et al.), dated October 21, 1997;

U.S. Patent No. 5,739,579 (Chiang et al.), dated April 14, 1998;

U.S. Patent No. 5,798,559 (Bothra et al.), dated August 25, 1998;

U.S. Patent No. 5,935,766 (Cheek et al.), dated August 10, 1999;

U.S. Patent No. 6,008,117 (Hong et al.), dated December 28, 1999.

Issues

1. Whether or not claims 1-7, 18-23, and 27 are obvious over Cheek et al. in view of Cohen et al. and further in view of Bothra et al. under 35 U.S.C. §103.

2. Whether or not claims 8-9 and 14-16 are obvious over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Chiang et al. under 35 U.S.C. §103.

3. Whether or not claims 12-13 are obvious over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Hong et al. under 35 U.S.C. §103.

4. Whether or not claims 10-11 are obvious over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of McCollum et al. under 35 U.S.C. §103.

Grouping of Claims:

Claim 1 is independent. Claims 2-23 and 27 depend on claim 1. The patentability of claims 2-23 and 27 are not separately argued. Therefore, claims 2-23 and 27 stand or fall with claim 1.

Arguments:

In the second paragraph on page 2 of the above-mentioned Office action, claims 1-7, 18-23, and 27 have been rejected as

being unpatentable over Cheek et al. in view of Cohen et al. and further in view of Bothra et al. under 35 U.S.C. § 103(a).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> at least one diffusion blocker disposed underneath said electrical connecting leads, said diffusion blocker at least one of impeding and preventing a diffusion of copper, said diffusion blocker configured as a blocker layer interrupted only in a region having said first contact holes formed therein, said blocker layer disposed between said first insulation layer and said second insulation layer. (Emphasis added.)

Cheek et al. show first and second insulating layers 130, 160 having respective contact holes. The first contact hole 140 within the first insulating layer 130 is filled with metal. The first contact hole 140 is covered with an aluminum metal line 150. The second contact hole 190 above the metal line 150 is filled with tungsten. The Examiner has already admitted that Cheek et al. do not teach that the second contact holes 190 are filled with copper in a whole-area manner and do not teach that a diffusion blocker layer is formed between the first and second insulating layers 130, 160 underneath the electrical connecting leads 150 (see the second paragraph on page 3 of the Office action).

However, the Examiner has stated that filling a contact hole in a whole-area manner is known from Cohen et al. As far as the diffusion blocker layer is concerned, the Examiner refers to Bothra et al.

It is true that Bothra et al. disclose a layer 116 which can be a silicon nitride layer. However, the purpose of layer 116 is different from the diffusion blocker layer (160) of the invention of the instant application. A person skilled in the art would not be motivated by the disclosure of Bothra et al. to include such a layer in the structure of Cheek et al., namely between the first and second insulation layers 130, 160 and underneath the metal line 150.

The semiconductor structure according to claim 1 of the instant application is optimized to prevent copper in the second contact hole (330) from diffusing downwardly to the semiconductor substrate. The blocking function is achieved by the combination of two measures. First, aluminum connection leads (250) are disposed above the first contact holes (170) (see page 17, line 8 of the specification). Second, a diffusion blocker layer (160) is disposed between the first and second insulating layers (150, 320). The diffusion

blocker layer (160) is only interrupted in a region having the first contact holes formed therein.

In Bothra et al., the layer 116 may include silicon nitride, which material is one of the preferred ones for the diffusion blocker layer (160) of the invention of the instant application. However, the function of the layer 116 in Bothra et al. is different from the function of the layer (160) in the invention of the instant application. The objective of Bothra et al. is to provide an air dielectric formation 180, which means that dielectric layers 120 and 140 are sacrificial oxide layers and will be removed from the semiconductor structure through an isotropic etch process. It can be clearly seen from the etch step depicted in Fig. 4 that the function of layer 116 is to prevent the isotropic etchant 162 from attacking all structures beneath the layer 116. Especially, silicon substrate 100 is protected from moisture that may cause corrosion or contamination (see column 4, lines 54 to 57 of Bothra et al.).

A person skilled in the art who seeks to improve the structure known from Cheek et al. looks for something to prevent contamination of copper into a semiconductor substrate. Bothra et al. do not suggest a mechanism for the prevention of copper diffusion. Rather, Bothra et al. show a silicon

nitride layer which is suitable to serve as an etch stop to prevent contamination and corrosion with moisture and the isotropic etchants. Bothra et al. do not mention that the layer 116 serves as a diffusion blocker to prevent copper from contaminating silicon substrate. A person skilled in the art has no intention to remove oxide 160 from the structure of Cheek. Consequently, a person skilled in the art would not consider Bothra et al. as a relevant document.

There are further indicia which support the position that the layer 116 has not been a point of consideration in the question of diffusion-blocking of copper in Bothra et al. For example, the contact hole filling 134, which is comparable to the contact hole filling (330) of the invention of the instant application, does not contain any copper. The contact hole filling 134 of Bothra et al. is formed of Tungsten (see column 7, line 20). The problem of preventing metal diffusion caused by a metal plug is solved by diffusion barrier layer 112 and 108. The layers 112 and 108, however, are situated within the contact holes 114, 110 within the first insulating layer 106. Diffusion layers 112, 108 are not disposed on the first insulating layer.

In summary, a person skilled in the art who attempts to prevent contamination of a silicon substrate from copper may

learn from Bothra et al. to place a diffusion layer, e.g. 112, 108, within each contact hole, and will learn that a silicon nitride layer 116 disposed on insulating layer 106 may be useful as an etch stop for removing sacrificial oxide in order to obtain air insulation. However, a person skilled in the art would not learn that the layer would serve as a diffusion blocker layer for above-disposed copper fillings of contact holes.

Consequently, Bothra et al. do not provide any hint toward placement of a diffusion blocker layer (160) within the structure of the invention of the instant application.

The Examiner has stated that if it is obvious to combine references for one reason it is obvious to combine references for all reasons (see the bottom of page 9 of the Office action). However, in establishing a *prima facie* case of obviousness, it is incumbent upon the Examiner to provide a reason why one of ordinary skill in the art would have been led to modify a prior art reference or to combine reference teachings to arrive at the claimed invention. Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Int. 1985). To this end, the requisite motivation must stem from some teaching, suggestion, or inference in the prior art as a whole or from the knowledge generally available to one of ordinary skill in

the art and not from the ***applicant's/appellant's*** disclosure. In this case, the Examiner did not point to anywhere in the cited references that provides a reason to combine the cited references in order to reach the invention of the instant application.

Cohen et al. disclose a layer 47 which may be formed of silicon nitride and covers an insulating layer 46. However, Cohen at al. do not use connection leads made of aluminum disposed above the diffusion blocker layer. Further, the barrier layer 47 is interrupted by the copper via 45 disposed above the layer 47. In contrast, in the invention of the instant application, the diffusion blocker layer (160) is interrupted by the first contact hole (170) which is below the diffusion blocker layer (160) and which would be comparable to contact 40 in Cohen et al. Cohen et al. solve the problem of copper diffusion by using diamond-like carbon material 46.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since claims 2-7, 18-23, and 27 are ultimately dependent on claim 1, they are believed to be patentable as well.

In the first paragraph on page 6 of the above-mentioned Office action, claims 8-9 and 14-16 have been rejected as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Chiang et al. under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claims 8-9 and 14-16 are ultimately dependent on claim 1, they are believed to be patentable as well.

In the fifth paragraph on page 7 of the above-mentioned Office action, claims 12-13 have been rejected as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Hong et al. under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claims 12-13 are ultimately dependent on claim 1, they are believed to be patentable as well.

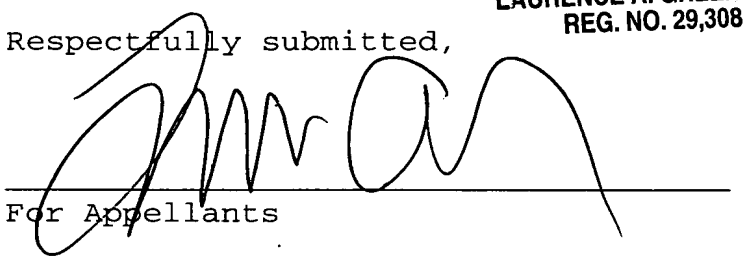
In the third paragraph on page 8 of the above-mentioned Office action, claims 10-11 have been rejected as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of McCollum et al. under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claims 10-11 are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the above, the honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308



For Appellants

YC/bb

Date: January 26, 2004
Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, Florida 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

Appendix - Appealed Claims:

1. An integrated electrical circuit, comprising:

a plurality of structure planes including at least one element structure plane;

electrically active elements disposed on said at least one element structure plane;

a first insulation layer disposed above said at least one element structure plane;

said first insulation layer having first contact holes disposed therein, and said first contact holes being filled with a metal;

a second insulation layer disposed above said first insulation layer;

said second insulation layer having second contact holes disposed therein and filled with electrical connecting leads, and said second contact holes being further filled with copper in a whole-area manner;

connection pieces disposed underneath said electrical connecting leads and above said first contact holes;

at least one diffusion blocker disposed underneath said electrical connecting leads, said diffusion blocker at least one of impeding and preventing a diffusion of copper, said diffusion blocker configured as a blocker layer interrupted only in a region having said first contact holes formed therein, said blocker layer disposed between said first insulation layer and said second insulation layer; and

said connection pieces being made of aluminum and covering said first contact holes and contacting said connection leads, and said connection pieces being covered by said second insulation layer.

2. The integrated electrical circuit according to claim 1, including a diffusion barrier for impeding a diffusion of copper disposed at at least one of a surface of said first contact holes and said connection pieces.

3. The integrated electrical circuit according to claim 1, wherein said electrical connecting leads have a copper content that is at least 10 percent by weight.

4. The integrated electrical circuit according to claim 1, wherein said insulation layer contains at least one substance selected from the group consisting of semiconductor oxides, semiconductor nitrides, fluorinated semiconductor oxides, fluorinated (amorphous) carbon, nitrides including boron nitride, polymers and polymer compounds including polyimides, polystyrenes, polyethylenes, polycarbonates, polybenzoxazole (PBO), benzocyclobutene (BCB), parylene, and fluoropolymers.

5. The integrated electrical circuit according to claim 1, wherein said blocker layer contains one of nitrogen, oxygen, fluorine, and a compound thereof.

6. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a nitride.

7. The integrated electrical circuit according to claim 6, wherein said blocker layer contains one of silicon nitride $Si_3N_4$ and tungsten silicon nitride $WSi_xN$.

8. The integrated electrical circuit according to claim 5, wherein said blocker layer contains an oxidized nitride.

9. The integrated electrical circuit according to claim 8, wherein said blocker layer contains at least one compound

selected from the group consisting of silicon oxynitride SiON, silicon boron oxynitride SiBON, titanium oxynitride $TiN_xO_y$, tantalum oxynitride $TaN_xO_y$, and tungsten oxynitride $WN_xO_y$.

10. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a fluorinated nitride.

11. The integrated electrical circuit as claimed in claim 10, wherein said blocker layer contains silicon fluorooxynitride SiOFN.

12. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a metal oxide.

13. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a material selected from the group consisting of titanium oxide $TiO_2$ and tantalum oxide $Ta_2O_5$.

14. The integrated electrical circuit according to claim 1, wherein said blocker layer has a thickness of between 50 nm and 800 nm.

15. The integrated electrical circuit according to claim 1, wherein said blocker layer is one of a plurality of blocker layers.

16. The integrated electrical circuit according to claim 15, wherein said blocker layers are disposed on different ones of said structure planes.

17. The integrated electrical circuit according to claim 15, wherein an extent to which said blocker layers impede diffusion and prevent diffusion differs.

18. The integrated electrical circuit according to claim 1, including at least one further diffusion blocker bearing on at least a portion of said electrical connecting leads.

19. The integrated electrical circuit according to claim 18, wherein said further diffusion blocker bears on at least one of side areas and lower edges of said portion of said electrical connecting leads.

20. The integrated electrical circuit according to claim 18, wherein said further diffusion blocker prevents bulk outdiffusion of copper into said first insulation layer.

21. The integrated electrical circuit according to claim 18, wherein an extent to which said blocker layer impedes diffusion is greater than that of said further diffusion blocker.

22. The integrated electrical circuit according to claim 18, wherein said blocker layer has a thickness greater than that of said further diffusion blocker.

23. The integrated electrical circuit according to claim 18, wherein a diffusion through said blocker layer is less than 10% of a diffusion through said further diffusion blocker.

27. The integrated electrical circuit according to claim 1, wherein said blocker layer includes an upper surface facing said second insulation layer and a lower surface facing said structure plane, said connection pieces being in contact with said upper surface of said blocker layer.

OIPE JC26 JAN 29 2004 PATENT & TRADEMARK OFFICE

Docket No.: GR 97 P 6457

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

MAIL STOP: APPEAL BRIEF-PATENTS

By: _____ Date: January 26, 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

| | | |
|---|---|---|
| Applic. No. | : | 09/595,860 Confirmation No.: 2756 |
| Inventor | : | Jörg Berthold et al. |
| Filed | : | June 16, 2000 |
| Title | : | Integrated Circuit Having a Diffusion Blocker Configured as a Blocker Layer and Connection Pieces Composed of Aluminum Covering Contact Holes and Methods for Fabricating the Same |
| TC/A.U. | : | 2811 |
| Examiner | : | Cuong Q. Nguyen |
| **Customer No.** | **:** | **24131** |

Hon. Commissioner for Patents
Alexandria, VA 22313-1450

## BRIEF ON APPEAL

S i r :

This is an appeal from the final rejection in the Office action dated September 10, 2003, finally rejecting claims 1-23 and 27.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $330.00 to cover the fee for filing the *Brief on Appeal*.

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 1-23 and 27 are rejected and are under appeal. Claims 25-26 were cancelled in an amendment filed July 1, 2002. Claims 24 and 28 are withdrawn from further consideration.

Status of Amendments:

No claims were amended after the final Office action. A *Notice of Appeal* was filed on November 24, 2003.

Summary of the Invention:

As stated in the first paragraph on page 1 of the specification of the instant application, the invention relates to an integrated electrical circuit having a plurality of structure planes, in which electrically active elements are situated on at least one element structure plane. At least

one insulation layer is disposed above the element structure plane and electrical connecting leads are disposed within and/or above the insulation layer. At least a portion of the connecting leads contains so much copper that copper is predominant for the properties of the connecting leads, and at least one diffusion blocker is disposed underneath the connecting leads, which diffusion blocker impedes and/or prevents the diffusion of copper.

Appellants explained on page 15 of the specification, line 10, that in all the figures of the drawing, sub-features and integral parts that correspond to one another bear the same reference symbol in each case. Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown an integrated electrical circuit having field-effect transistors 20, 30 and 40 that are situated on a semiconductor substrate 10 preferably composed of silicon. The field-effect transistors 20, 30 and 40 each have source and drain regions 50, 60, 70, 80, 90 and 100 and also gate electrodes 120, 130 and 140.

Appellants further explained on page 15 of the specification, line 21, that an insulation layer 150 is situated between the field-effect transistors 20, 30 and 40 and also above the source and drain regions 50, 60, 70, 80, 90 and 100 and also

between the gate electrodes 120, 130 and 140. The insulation layer 150 may be formed, in particular, by an intermediate oxide, for example a flowable planarization oxide such as borophosphorus silicate glass (BPSG). The intermediate oxide can be replaced by any other insulating material. However, the use of borophosphorus silicate glass has the particular advantage that, on account of its flowability, it may be possible to dispense with a process of chemical mechanical planarization for the purpose of producing a planar surface.

It is outlined on page 16 of the specification, line 8, that a blocker layer 160 having a thickness of 150 nm and made, for example, of silicon oxynitride SiON is disposed above the insulation layer 150. The blocker layer 160 is disposed above the entire surface of the semiconductor substrate 10 and is interrupted only in a region of contact holes 170, 180, 190, 200, 210 and 220. The contact holes 170, 180, 190, 200, 210 and 220 are preferably filled in a whole-area manner with a conductive material, for example a metal, preferably tungsten or a tungsten alloy.

It is also outlined on page 16 of the specification, line 18, that, as can be discerned from Fig. 2, an adhesion layer 165 having a thickness of approximately 100 nm and made of a titanium/titanium nitride alloy is situated between a tungsten

filling 230 of a contact hole 240 and the layers which bound the contact hole, that is to say the insulation layer 150 and the blocker layer 160. The adhesion layer 165 serves as a seeding layer for subsequent deposition operations, in particular for the filling of the contact holes 170, 180, 190, 200, 210, 220 and 240 with tungsten, for example. In addition, the adhesion layer 165 protects the material underneath the bottom of the contact hole.

It is set forth on page 17 of the specification, line 4, that above the contact holes 170, 180, 190, 200, 210, 220 and 240, connection pieces 250, 260, 270, 280, 290, 300 and 310 are situated directly on the blocker layer 160. The connection pieces being made of a material which combines a high conductivity with a minor diffusion tendency, for example aluminum.

Appellants also set forth on page 17 of the specification, line 11, that a further insulation layer 320, which is also referred to as an intermetal oxide, is situated above and between the connection pieces 250, 260, 270, 280, 290, 300 and 310. However, it is not necessary for the insulation layer 320 to be composed of an oxide, although it is technologically particularly expedient for it to be composed of a semiconductor oxide such as, for example, $SiO_2$ formed by a TEOS

(tetraethyl orthosilicate = $SiO(OC_2H_5)_4$) method. As an alternative, it is possible for the insulation layer 320 (that is to say the intermetal oxide in this case) to be deposited for example by a chemical vapor deposition (CVD) method. In all of the cases mentioned, the production of the insulation layer 320 can be integrated without difficulty in the process for fabricating the electrical circuit.

Appellants outlined on page 18 of the specification, line 1, that contact holes 330, 340, 350, 360 and 370 are likewise etched into the insulation layer 320.

Appellants further outlined on page 18 of the specification, line 4, that the contact holes 330, 340, 350, 360 and 370 are filled with tungsten or copper in a whole-area manner. Above the insulation layer 320, connection pieces 390 and 400 and also an interconnect 410 made of copper are situated in a further insulation layer 380.

It is also stated on page 18 of the specification, line 10, that contact holes 420 and 430 are likewise situated in the insulation layer 380 and are in turn filled with tungsten or copper in a whole-area manner.

Appellants also explained on page 18 of the specification, line 14, that connection pieces 440 and 450 made of copper are likewise disposed above the contact holes 420 and 430. The connection pieces 440, 450 are situated in an intermetal dielectric 460 which lies above the insulation layer 380 and is composed of a silicon oxide $SiO_2$, for example.

Appellants outlined in the last paragraph on page 18 of the specification, line 20, that the integrated electrical circuit of this type can be produced in the manner explained below. The field-effect transistors 20, 30 and 40 with the source and drain regions 50, 60, 70, 80, 90 and 100 and also with the gate electrodes 120, 130 and 140 are fabricated in a known manner in the region of a main area of the semiconductor substrate 10.

Appellants outlined on page 19 of the specification, line 1, that this is followed by the production of the insulation layer 150, for example by the flowing of a flowable planarization oxide such as borophosphorus silicate glass (BPSG) or by a coating method such as plasma-enhanced CVD: PECVD (plasma enhanced chemical vapor deposition) method.

Appellants further outlined on page 19 of the specification, line 7, that the blocker layer 160 having a thickness of

approximately 100 nm is coated onto the insulation layer 150. The blocker layer 160 - for example made of silicon oxynitride SiON - may preferably be fabricated by a PECVD method. A significant advantage of the PECVD method is that it can be carried out even at temperatures of below 500° C. In this case, free radicals are produced in a plasma. These are silicon, oxide and nitride radicals in the case of an SiON layer being deposited. Silane ($SiH_4$), ammonia ($NH_3$) and oxygen are used for carrying out the method. The blocker layer 160 is deposited at a pressure in the range of from about 20 to 100 Pa, preferably approximately 30 Pa, and a temperature below 500° C, preferably about 300° C.

It is set forth in the last paragraph on page 19 of the specification, line 21, that, afterwards, the contact holes 170, 180, 190, 200, 210, 220 and 240 are etched into the insulation layer 150 and into the blocker layer 160, preferably by a dry etching method in a reactive plasma. An example of an etchant used is a gas mixture comprising $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$.

Appellants stated on page 20 of the specification, line 1, that the adhesion layer 165 having a thickness of approximately 100 nm and made of a titanium/titanium nitride alloy is subsequently deposited. The contact holes 170, 180,

190, 200, 210, 220 and 240 are thereupon filled with tungsten or copper.

Appellants further stated on page 20 of the specification, line 6, that the connection pieces 250, 260, 270, 280, 290, 300 and 310 that may also be connecting elements, are subsequently applied for example by the sputtering and subsequent patterning of a metal layer.

It is also set forth on page 20 of the specification, line 11, that a patterning process according to a conventional photolithographic method patterns that part of the adhesion layer 165 which lies above the blocker layer 160 and equally the connection pieces 250, 260, 270, 280, 290, 300 and 310.

As described on page 20 of the specification, line 16, the insulation layer 320 is then deposited onto the blocker layer 160 and the connection pieces 250, 260, 270, 280, 290, 300 and 310 by a suitable deposition method - such as plasma enhanced chemical vapor deposition (PECVD).

Appellants described in the last paragraph on page 20 of the specification, line 21, that the contact holes 330, 340, 350, 360 and 370 are then etched into the insulation layer 320 preferably by a dry etching method in a reactive plasma. An

example of a suitable etchant used is a gas mixture containing $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$.

Appellants explained on page 21 of the specification, line 1, that the connection pieces 390 and 400 made of copper and also an interconnect 410, which serves for connecting the contact holes 350 and 360 and is likewise composed of copper, are produced in the manner explained below. A copper layer having a thickness of from 300 nm to 600 nm is applied to the layer 320 by a sputtering method. A resist mask is then applied and patterned by photolithographic process steps.

Appellants further explained on page 21 of the specification, lien 9, that the insulation layer 380 is subsequently applied. The contact holes 420 and 430 are then etched into the insulation layer 380 preferably by a dry etching method in a reactive plasma. An example of an etchant used is once again a gas mixture containing $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$. The contact holes 420 and 430 are subsequently filled with copper. The connection pieces 440 and 450 made of copper are then applied to the contact holes 420 and 430.

It is also stated on page 21 of the specification, line 18, that a further plane 460 formed for example by an intermetal dielectric such as $SiO_2$ is subsequently applied.

It is outlined in the last paragraph on page 21 of the specification, line 21, that, in the case of a second embodiment of the integrated electrical circuit illustrated in Fig. 3, field-effect transistors 520, 530 and 540 are situated on a semiconductor substrate 510 preferably composed of silicon. The field-effect transistors 520, 530 and 540 each have source and drain regions 550, 560, 570, 580, 590 and 600 and also gate electrodes 620, 630 and 640.

Appellants stated on page 22 of the specification, line 4, that an insulation layer 650 is situated between the field-effect transistors 520, 530 and 540 and also above the source and drain regions and also the gate electrodes. The insulation layer 650 may be composed, in particular, of an intermediate oxide, for example a flowable planarization oxide such as borophosphorus silicate glass (BPSG). The intermediate oxide may be replaced by any other insulating material. However, the use of borophosphorus silicate glass has the particular advantage that, on account of its flowability, it may be possible to dispense with a process of chemical mechanical planarization for the purpose of producing a planar surface.

Appellants set forth in the last paragraph on page 22 of the specification, line 16, that a blocker layer 660 having a thickness of 150 nm and made of silicon oxynitride SiON is disposed above the insulation layer 650. The blocker layer 660 is disposed above the entire surface of the semiconductor substrate 510 and encloses the connection pieces 750, 760, 770, 780, 790 and 800 located in the region of contact holes 670, 680, 690, 700, 710, 720 and 740. The contact holes 670, 680, 690, 700, 710 and 720 are preferably filled in a whole-area manner with a conductive material, for example a metal, preferably tungsten or a tungsten alloy. The connection pieces 750, 760, 770, 780, 790, 800 and 810 are composed of a material that combines a high conductivity with a minor diffusion tendency, for example aluminum.

Appellants explained on page 23 of the specification, line 4, that, as can be discerned from Fig. 4, an adhesion layer 665 having a thickness of approximately 100 nm and made of a titanium/titanium nitride alloy is situated between the tungsten filling 730 of a contact hole 740 and the layer which bounds the contact hole, that is to say in this case the insulation layer 650. The adhesion layer 665 serves as a seeding layer for subsequent deposition operations, in particular for the filling of the contact holes 670, 680, 690, 700, 710, 720 and 740 with tungsten, for example. In

addition, the adhesion layer 665 protects the material underneath the bottom of the contact hole.

It is set forth in the last paragraph on page 23 of the specification, line 16, that a further insulation layer 820, which is also referred to as an intermetal oxide, is situated above and between the connection pieces 750, 760, 770, 780, 790, 800. However, it is not necessary for the insulation layer 820 to be composed of an oxide, although it is technologically particularly expedient for it to be composed of a semiconductor oxide such as, for example, $SiO_2$ formed by a TEOS (tetraethyl orthosilicate = $SiO(OC_2H_5)_4$) method. As an alternative, it is possible for the insulation layer 820 (that is to say the intermetal oxide in this case) to be deposited for example by a chemical vapor deposition (CVD) method. In all of the cases mentioned, the production of the insulation layer 820 can be integrated without difficulty in the process for fabricating the electrical circuit.

Appellants explained on page 24 of the specification, line 5, that contact holes 830, 840, 850 and 860 are likewise etched into the insulation layer 820.

Appellants further explained on page 24 of the specification, line 8, that the contact holes 830, 840, 850 and 860 are

filled with tungsten or copper in a whole-area manner. Above the insulation layer 820, connection pieces 890 and 890 and also an interconnect 910 made of copper are situated in a further insulation layer 880.

It is also stated on page 24 of the specification, line 24, that contact holes 920 and 930 are likewise situated in the insulation layer 880 and are in turn filled with tungsten or copper in a whole-area manner.

Appellants also described on page 24 of the specification, line 18, that connection pieces 940 and 950 made of copper are likewise disposed above the contact holes 920 and 930.

It is set forth in the last paragraph on page 24 of the specification, line 21, that an integrated electrical circuit of this type can be produced in the manner explained below. The field-effect transistors 520, 530 and 540 with the source and drain regions 550, 560, 570, 580, 590 and 600 and also with the gate electrodes 620, 630 and 640 are fabricated in a known manner in the region of a main area of a semiconductor substrate 510.

Appellants outlined on page 25 of the specification, line 1, that this is followed by the production of the insulation

layer 650, for example by the flowing of a flowable planarization oxide such as borophosphorus silicate glass (BPSG) or by a coating method such as plasma-enhanced CVD: PECVD (plasma enhanced chemical vapor deposition) method.

Appellants further outlined on page 25 of the specification, line 8, that, afterwards, the contact holes 670, 680, 690, 700, 710, 720 and 740 are etched into the insulation layer 650, preferably by a dry etching method in a reactive plasma. An example of an etchant used is a gas mixture containing $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$.

It is also stated on page 25 of the specification, line 14, that the adhesion layer 665 having a thickness of approximately 100 nm and made of a titanium/titanium nitride alloy is subsequently deposited. The contact holes 670, 680, 690, 700, 710, 720 and 740 are thereupon filled with tungsten or copper.

Appellants described in the last paragraph on page 25 of the specification, line 19, that the connection pieces 750, 760, 770, 780, 790 and 800, which may also be connecting elements, are subsequently applied for example by the sputtering and subsequent patterning of a metal layer made of aluminum or an aluminum alloy, for example. A patterning process according

to a conventional photolithographic method patterns that part of the adhesion layer 665 which lies above the insulation layer 650 and equally the connection pieces 750, 760, 770, 780, 790 and 800.

Appellants outlined on page 26 of the specification, line 2, that the blocker layer 660 having a thickness of approximately 100 nm is then coated onto the insulation layer 650 and the connection pieces 750, 760, 770, 780, 790 and 800. The blocker layer 660 - for example made of silicon oxynitride SiON - may preferably be fabricated by a PECVD method. A significant advantage of the PECVD method is that it can be carried out even at temperatures of below 500° C. In this case, free radicals are produced in a plasma. These are silicon, oxide and nitride radicals in the case of an SiON layer being deposited. Silane ($SiH_4$), ammonia ($NH_3$) and oxygen are used for carrying out the method. The blocker layer 660 is preferably deposited at a pressure in the range of about 20 to 100 Pa, ideally at about 30 Pa, and a temperature of below 500° C, preferably about 300° C.

Appellants further outlined on page 26 of the specification, line 17, that the connection pieces 750, 760, 770, 780, 790 and 800 are subsequently produced by applying and subsequently patterning a metal layer. The insulation layer 820 is then

deposited onto the blocker layer 660 and the connection pieces 750, 760, 770, 780, 790, 800 and 810 by a suitable deposition method such as chemical vapor deposition (CVD). The contact holes 830, 840, 850, 860 and 870 are then etched into the insulation layer 820. An example of an etchant used is a gas mixture containing $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$.

It is set forth in the first paragraph on page 27 of the specification, line 1, that the connection pieces 890 and 900 made of copper and also an interconnect 910, which serves for connecting the contact holes 850 and 860 and is likewise composed of copper, are produced in the manner explained below. A copper layer having a thickness of from 300 nm to 600 nm is applied to the insulation layer 820 by a sputtering method. A resist mask is then applied and patterned by photolithographic process steps.

As further outlined on page 27 of the specification, line 9, the further insulation layer 880 is then deposited. The contact holes 920 and 930 are then etched into the insulation layer 880 preferably by a dry etching method in a reactive plasma. An example of an etchant used is again a gas mixture containing $CHF_3$ and $O_2$ or containing $CHF_3$ and $CF_4$. The contact holes 920 and 930 are subsequently filled with copper.

Connection pieces 940 and 950 made of copper are then applied to the contact holes 920 and 930.

Appellants stated in the last paragraph on page 27 of the specification, line 18, that the intermetal dielectric 960, for example made of silicon oxide $SiO_2$, is subsequently applied.

References Cited:

U.S. Patent No. 5,552,627 (McCollum et al.), dated September 3, 1996;

U.S. Patent No. 5,679,269 (Cohen et al.), dated October 21, 1997;

U.S. Patent No. 5,739,579 (Chiang et al.), dated April 14, 1998;

U.S. Patent No. 5,798,559 (Bothra et al.), dated August 25, 1998;

U.S. Patent No. 5,935,766 (Cheek et al.), dated August 10, 1999;

U.S. Patent No. 6,008,117 (Hong et al.), dated December 28, 1999.

Issues

1. Whether or not claims 1-7, 18-23, and 27 are obvious over Cheek et al. in view of Cohen et al. and further in view of Bothra et al. under 35 U.S.C. §103.

2. Whether or not claims 8-9 and 14-16 are obvious over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Chiang et al. under 35 U.S.C. §103.

3. Whether or not claims 12-13 are obvious over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Hong et al. under 35 U.S.C. §103.

4. Whether or not claims 10-11 are obvious over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of McCollum et al. under 35 U.S.C. §103.

Grouping of Claims:

Claim 1 is independent. Claims 2-23 and 27 depend on claim 1. The patentability of claims 2-23 and 27 are not separately argued. Therefore, claims 2-23 and 27 stand or fall with claim 1.

Arguments:

In the second paragraph on page 2 of the above-mentioned Office action, claims 1-7, 18-23, and 27 have been rejected as

being unpatentable over Cheek et al. in view of Cohen et al. and further in view of Bothra et al. under 35 U.S.C. § 103(a).

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> at least one diffusion blocker disposed underneath said electrical connecting leads, said diffusion blocker at least one of impeding and preventing a diffusion of copper, said diffusion blocker configured as a blocker layer interrupted only in a region having said first contact holes formed therein, said blocker layer disposed between said first insulation layer and said second insulation layer. (Emphasis added.)

Cheek et al. show first and second insulating layers 130, 160 having respective contact holes. The first contact hole 140 within the first insulating layer 130 is filled with metal. The first contact hole 140 is covered with an aluminum metal line 150. The second contact hole 190 above the metal line 150 is filled with tungsten. The Examiner has already admitted that Cheek et al. do not teach that the second contact holes 190 are filled with copper in a whole-area manner and do not teach that a diffusion blocker layer is formed between the first and second insulating layers 130, 160 underneath the electrical connecting leads 150 (see the second paragraph on page 3 of the Office action).

However, the Examiner has stated that filling a contact hole in a whole-area manner is known from Cohen et al. As far as the diffusion blocker layer is concerned, the Examiner refers to Bothra et al.

It is true that Bothra et al. disclose a layer 116 which can be a silicon nitride layer. However, the purpose of layer 116 is different from the diffusion blocker layer (160) of the invention of the instant application. A person skilled in the art would not be motivated by the disclosure of Bothra et al. to include such a layer in the structure of Cheek et al., namely between the first and second insulation layers 130, 160 and underneath the metal line 150.

The semiconductor structure according to claim 1 of the instant application is optimized to prevent copper in the second contact hole (330) from diffusing downwardly to the semiconductor substrate. The blocking function is achieved by the combination of two measures. First, aluminum connection leads (250) are disposed above the first contact holes (170) (see page 17, line 8 of the specification). Second, a diffusion blocker layer (160) is disposed between the first and second insulating layers (150, 320). The diffusion

blocker layer (160) is only interrupted in a region having the first contact holes formed therein.

In Bothra et al., the layer 116 may include silicon nitride, which material is one of the preferred ones for the diffusion blocker layer (160) of the invention of the instant application. However, the function of the layer 116 in Bothra et al. is different from the function of the layer (160) in the invention of the instant application. The objective of Bothra et al. is to provide an air dielectric formation 180, which means that dielectric layers 120 and 140 are sacrificial oxide layers and will be removed from the semiconductor structure through an isotropic etch process. It can be clearly seen from the etch step depicted in Fig. 4 that the function of layer 116 is to prevent the isotropic etchant 162 from attacking all structures beneath the layer 116. Especially, silicon substrate 100 is protected from moisture that may cause corrosion or contamination (see column 4, lines 54 to 57 of Bothra et al.).

A person skilled in the art who seeks to improve the structure known from Cheek et al. looks for something to prevent contamination of copper into a semiconductor substrate. Bothra et al. do not suggest a mechanism for the prevention of copper diffusion. Rather, Bothra et al. show a silicon

nitride layer which is suitable to serve as an etch stop to prevent contamination and corrosion with moisture and the isotropic etchants. Bothra et al. do not mention that the layer 116 serves as a diffusion blocker to prevent copper from contaminating silicon substrate. A person skilled in the art has no intention to remove oxide 160 from the structure of Cheek. Consequently, a person skilled in the art would not consider Bothra et al. as a relevant document.

There are further indicia which support the position that the layer 116 has not been a point of consideration in the question of diffusion-blocking of copper in Bothra et al. For example, the contact hole filling 134, which is comparable to the contact hole filling (330) of the invention of the instant application, does not contain any copper. The contact hole filling 134 of Bothra et al. is formed of Tungsten (see column 7, line 20). The problem of preventing metal diffusion caused by a metal plug is solved by diffusion barrier layer 112 and 108. The layers 112 and 108, however, are situated within the contact holes 114, 110 within the first insulating layer 106. Diffusion layers 112, 108 are not disposed on the first insulating layer.

In summary, a person skilled in the art who attempts to prevent contamination of a silicon substrate from copper may

learn from Bothra et al. to place a diffusion layer, e.g. 112, 108, within each contact hole, and will learn that a silicon nitride layer 116 disposed on insulating layer 106 may be useful as an etch stop for removing sacrificial oxide in order to obtain air insulation. However, a person skilled in the art would not learn that the layer would serve as a diffusion blocker layer for above-disposed copper fillings of contact holes.

Consequently, Bothra et al. do not provide any hint toward placement of a diffusion blocker layer (160) within the structure of the invention of the instant application.

The Examiner has stated that if it is obvious to combine references for one reason it is obvious to combine references for all reasons (see the bottom of page 9 of the Office action). However, in establishing a *prima facie* case of obviousness, it is incumbent upon the Examiner to provide a reason why one of ordinary skill in the art would have been led to modify a prior art reference or to combine reference teachings to arrive at the claimed invention. Ex parte Clapp, 227 USPQ 972, 973 (Bd. Pat. App. & Int. 1985). To this end, the requisite motivation must stem from some teaching, suggestion, or inference in the prior art as a whole or from the knowledge generally available to one of ordinary skill in

the art and not from the ***applicant's/appellant's*** disclosure. In this case, the Examiner did not point to anywhere in the cited references that provides a reason to combine the cited references in order to reach the invention of the instant application.

Cohen et al. disclose a layer 47 which may be formed of silicon nitride and covers an insulating layer 46. However, Cohen at al. do not use connection leads made of aluminum disposed above the diffusion blocker layer. Further, the barrier layer 47 is interrupted by the copper via 45 disposed above the layer 47. In contrast, in the invention of the instant application, the diffusion blocker layer (160) is interrupted by the first contact hole (170) which is below the diffusion blocker layer (160) and which would be comparable to contact 40 in Cohen et al. Cohen et al. solve the problem of copper diffusion by using diamond-like carbon material 46.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since claims 2-7, 18-23, and 27 are ultimately dependent on claim 1, they are believed to be patentable as well.

In the first paragraph on page 6 of the above-mentioned Office action, claims 8-9 and 14-16 have been rejected as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Chiang et al. under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claims 8-9 and 14-16 are ultimately dependent on claim 1, they are believed to be patentable as well.

In the fifth paragraph on page 7 of the above-mentioned Office action, claims 12-13 have been rejected as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Hong et al. under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claims 12-13 are ultimately dependent on claim 1, they are believed to be patentable as well.

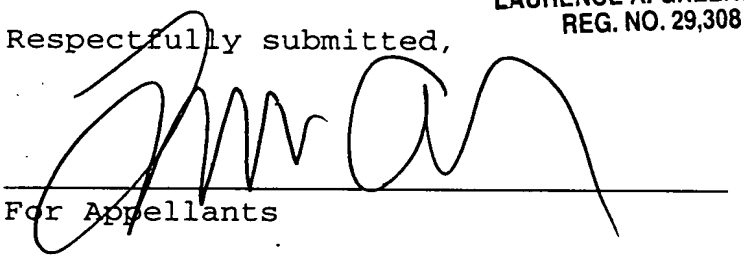
In the third paragraph on page 8 of the above-mentioned Office action, claims 10-11 have been rejected as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of McCollum et al. under 35 U.S.C. § 103(a).

As discussed above, claim 1 is believed to be patentable over the art. Since claims 10-11 are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the above, the honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

LAURENCE A. GREENBERG
REG. NO. 29,308



For Appellants

YC/bb

Date: January 26, 2004
Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, Florida 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

Appendix - Appealed Claims:

1. An integrated electrical circuit, comprising:

a plurality of structure planes including at least one element structure plane;

electrically active elements disposed on said at least one element structure plane;

a first insulation layer disposed above said at least one element structure plane;

said first insulation layer having first contact holes disposed therein, and said first contact holes being filled with a metal;

a second insulation layer disposed above said first insulation layer;

said second insulation layer having second contact holes disposed therein and filled with electrical connecting leads, and said second contact holes being further filled with copper in a whole-area manner;

connection pieces disposed underneath said electrical connecting leads and above said first contact holes;

at least one diffusion blocker disposed underneath said electrical connecting leads, said diffusion blocker at least one of impeding and preventing a diffusion of copper, said diffusion blocker configured as a blocker layer interrupted only in a region having said first contact holes formed therein, said blocker layer disposed between said first insulation layer and said second insulation layer; and

said connection pieces being made of aluminum and covering said first contact holes and contacting said connection leads, and said connection pieces being covered by said second insulation layer.

2. The integrated electrical circuit according to claim 1, including a diffusion barrier for impeding a diffusion of copper disposed at at least one of a surface of said first contact holes and said connection pieces.

3. The integrated electrical circuit according to claim 1, wherein said electrical connecting leads have a copper content that is at least 10 percent by weight.

4. The integrated electrical circuit according to claim 1, wherein said insulation layer contains at least one substance selected from the group consisting of semiconductor oxides, semiconductor nitrides, fluorinated semiconductor oxides, fluorinated (amorphous) carbon, nitrides including boron nitride, polymers and polymer compounds including polyimides, polystyrenes, polyethylenes, polycarbonates, polybenzoxazole (PBO), benzocyclobutene (BCB), parylene, and fluoropolymers.

5. The integrated electrical circuit according to claim 1, wherein said blocker layer contains one of nitrogen, oxygen, fluorine, and a compound thereof.

6. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a nitride.

7. The integrated electrical circuit according to claim 6, wherein said blocker layer contains one of silicon nitride $Si_3N_4$ and tungsten silicon nitride $WSi_xN$.

8. The integrated electrical circuit according to claim 5, wherein said blocker layer contains an oxidized nitride.

9. The integrated electrical circuit according to claim 8, wherein said blocker layer contains at least one compound

selected from the group consisting of silicon oxynitride SiON, silicon boron oxynitride SiBON, titanium oxynitride $TiN_xO_y$, tantalum oxynitride $TaN_xO_y$, and tungsten oxynitride $WN_xO_y$.

10. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a fluorinated nitride.

11. The integrated electrical circuit as claimed in claim 10, wherein said blocker layer contains silicon fluorooxynitride SiOFN.

12. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a metal oxide.

13. The integrated electrical circuit according to claim 5, wherein said blocker layer contains a material selected from the group consisting of titanium oxide $TiO_2$ and tantalum oxide $Ta_2O_5$.

14. The integrated electrical circuit according to claim 1, wherein said blocker layer has a thickness of between 50 nm and 800 nm.

15. The integrated electrical circuit according to claim 1, wherein said blocker layer is one of a plurality of blocker layers.

16. The integrated electrical circuit according to claim 15, wherein said blocker layers are disposed on different ones of said structure planes.

17. The integrated electrical circuit according to claim 15, wherein an extent to which said blocker layers impede diffusion and prevent diffusion differs.

18. The integrated electrical circuit according to claim 1, including at least one further diffusion blocker bearing on at least a portion of said electrical connecting leads.

19. The integrated electrical circuit according to claim 18, wherein said further diffusion blocker bears on at least one of side areas and lower edges of said portion of said electrical connecting leads.

20. The integrated electrical circuit according to claim 18, wherein said further diffusion blocker prevents bulk outdiffusion of copper into said first insulation layer.

21. The integrated electrical circuit according to claim 18, wherein an extent to which said blocker layer impedes diffusion is greater than that of said further diffusion blocker.

22. The integrated electrical circuit according to claim 18, wherein said blocker layer has a thickness greater than that of said further diffusion blocker.

23. The integrated electrical circuit according to claim 18, wherein a diffusion through said blocker layer is less than 10% of a diffusion through said further diffusion blocker.

27. The integrated electrical circuit according to claim 1, wherein said blocker layer includes an upper surface facing said second insulation layer and a lower surface facing said structure plane, said connection pieces being in contact with said upper surface of said blocker layer.